This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (original) A chip scale integrated circuit chip package comprising a die mounted by flip chip interconnection to a package substrate, the package substrate being a laminate comprising a dielectric layer having a single conductive trace layer on a first surface thereof and an active ground plane overlying a second surface thereof, wherein the ground plane is electrically connected to ground sites at the first surface of the dielectric layer through openings in the dielectric layer, and wherein second level interconnects are on the first surface of the dielectric layer, and the die is mounted on the first surface of the dielectric layer.

2. (original) The package of claim 1 wherein the openings in the dielectric layer are filled with an electrically conductive material.

3. (original) The package of claim 2 wherein the electrically conductive material comprises a solder.

4. (original) The package of claim 2 wherein the electrically conductive material comprises a conductive ink.

5. (original) The package of claim 2 wherein the electrically conductive material comprises a metal-filled epoxy.

6. (original) The package of claim 5 wherein the electrically conductive material comprises a silver-filled epoxy.

7. (original) The package of claim 1 wherein the ground plane comprises an electrically conductive film overlying the second surface of the dielectric layer.

8. (original) The package of claim 1 wherein the openings in the dielectric layer are filled with an electrically conductive material and the ground plane and the electrically conductive fill material are substantially the same material.

9. (original) The package of claim 1 wherein the openings in the dielectric layer are filled with an electrically conductive material and the ground plane is formed of a material different from the electrically conductive fill material.

10. (original) The package of claim 1 wherein the ground plane is disposed directly upon the surface of the dielectric layer on the dielectric side.

11. (original) The package of claim 1 wherein the ground plane is disposed upon a conductive film formed over the dielectric side of the dielectric layer.

12. (original) The package of claim 1 wherein the ground plane is disposed upon an adhesive layer formed over the dielectric side of the dielectric layer.

13. (original) The package of claim 12 wherein the adhesive layer comprises an electrically insulating adhesive layer.

14. (original) The package of claim1 wherein the ground plane comprises a metal.

15. (original) The package of claim 14 wherein the ground plane comprises aluminum.

16. (original) The package of claim 14 wherein the ground plane comprises nickel.

17. (original) The package of claim 14 wherein the ground plane comprises copper.

18. (original) The package of claim 1 wherein a gap between the die and the substrate is at least partly filled with a die attach material.

19. (original) The package of claim 18 wherein the die attach material comprises an epoxy.

20. (original) The package of claim 1 wherein the die is provided with interconnection bumps affixed to an arrangement of connection sites in a first surface of the die, and the conductive trace layer is provided with a complementary arrangement of interconnect sites, and the flip chip interconnection is a solid state interconnection.

21. (original) The package of claim 1 wherein the die is attached at about the center of the first side of the substrate, and solder balls for second level interconnections are located nearer the periphery of the first side of the substrate.

22. (original) The package of claim 1 wherein the electrical traces are formed within an interconnect layer in the first surface of the package substrate, and the traces fan outward from the interconnect pads to the solder ball attachment sites.

23. (original) The package of claim 1 wherein at least some of the traces are constructed as coplanar waveguides, each comprising ground lines alongside a signal line on a planar dielectric material.

24. (original) A method for manufacturing an integrated circuit chip package, comprising

providing a substrate having a circuit side and a dielectric side, the substrate comprising an electrically insulating layer and a patterned electrically conductive layer, the substrate further including vias through the insulating layer opening on an exposed surface of the insulating layer;

affixing a semiconductor die onto the circuit side of the substrate and forming a flip chip interconnection;

filling the vias with an electrically conductive material;

applying an electrically conductive layer onto the exposed surface of the electrically insulating material, the electrically conductive layer covering at least a portion of the dielectric side of the substrate; and

curing the electrically insulating material.

25. (original) The method of claim 24 wherein filling the vias comprises applying a curable electrically conductive material in the vias.

26. (original) The method of claim 25 wherein applying an electrically conductive layer comprises applying a curable conductive adhesive.

27. (original) The method of claim 25 wherein applying an electrically conductive layer comprises applying a metal sheet.

28. (original) The method of claim 25 wherein affixing the semiconductor die comprises providing a die having interconnection bumps affixed to an arrangement of connection sites in a first surface of thereof, and forming the flip chip interconnection comprises apposing the interconnect face of the die with interconnect sites on a first side of the package substrate and bringing the interconnect bumps into contact with a complementary arrangement of interconnect sites on the conductive trace layer under conditions of pressure and temperature that promote bonding of the bumps on the interconnect sites without melting the material of the bumps or of the interconnect sites on the conductive trace layer.

29. (original) The method of claim 25, further comprising attaching second level interconnect solder balls onto second level interconnect sites on the conductive trace layer.

30. (original) The method of claim 25 wherein providing the substrate comprises providing a substrate comprising a patterned electrically conductive layer and an electrically insulating layer.

31. (original) A method for manufacturing an integrated circuit chip package, comprising

providing a substrate including a dielectric layer having first and second surfaces and a patterned electrically conductive film on the first surface, the side of the substrate having the patterned conductive film being a circuit side of the substrate, and the side of the substrate having the second surface being a dielectric side of the substrate, the substrate having vias through the dielectric layer opening on the second surface;

affixing a semiconductor die onto the circuit side of the substrate and forming a flip chip interconnection;

applying an electrically conductive material onto the dielectric side of the substrate, filling the vias and covering at least a portion of the dielectric side of the substrate; and

curing the electrically conductive material.

32. (original) The method of claim 31 wherein applying the electrically conductive material comprises applying a curable electrically conductive adhesive.

33. (original) The method of claim 31 wherein applying the electrically conductive material comprises applying a conductive ink.

34. (original) The method of claim 31 wherein the substrate is provided as a single metal layer tape substrate, the method further comprising supporting the tape on a stage with at least one side of the substrate exposed for subsequent treatment.

35. (original) The method of claim 31, further comprising affixing second level interconnect solder balls onto the circuit side of the substrate.

36. (original) The method of claim 31 wherein the die is provided with interconnection bumps affixed to an arrangement of connection sites in a first surface of the die, and the flip chip interconnection is formed by apposing the interconnect face of the die with interconnect sites on the circuit side of the substrate and bringing the interconnect bumps into contact with a complementary arrangement of interconnect sites on the patterned conductive film under conditions of pressure and temperature that promote bonding of the bumps on the interconnect sites without melting the material of the bumps or of the interconnect sites on the conductive trace layer.

37. (original) The method of claim 31, further comprising applying a metal sheet onto an exposed surface of the curable electrically conductive material.

38. (original) The method of claim 37 wherein applying a metal sheet comprises applying a copper sheet.

39. (original) The method of claim 37 wherein applying a metal sheet comprises applying an aluminum sheet.

40. (original) The method of claim 37 wherein the electrically conductive material comprises a curable adhesive, and wherein the metal sheet is applied prior to curing the electrically conductive material.

41. (original) A method for manufacturing an integrated circuit chip package, comprising

providing a substrate including a dielectric layer having first and second surfaces, and having an electrically insulating adhesive layer on the second surface and a patterned electrically conductive layer on the first surface, the side of the substrate having the patterned conductive layer being a "circuit side" of the substrate, and the side of the substrate having the electrically insulating adhesive layer being the "dielectric side" of the substrate, the substrate having vias through the insulating layer and the dielectric layer opening on the exposed surface of the insulating layer;

affixing a semiconductor die onto the circuit side of the substrate and forming a flip chip interconnection;

filling the vias with an electrically conductive material;

applying an electrically conductive layer onto the exposed surface of the electrically insulating material, the electrically conductive layer making electrical contact with the electrically conductive material in the vias, and thereby with selected traces in the patterned electrically conductive layer, and covering at least a portion of the dielectric side of the substrate; and

curing the electrically insulating material.